

## Dual 4-Channel Analog Data Selector

The MC14529B analog data selector is a dual 4-channel or single 8-channel device depending on the input coding. The device is suitable for digital as well as analog application, including various one-of-four and one-of-eight data selector functions. Since the device has bidirectional analog characteristics it can also be used as a dual binary to 1-of-4 or a binary to 1-of-8 decoder.

- Data Paths Are Bidirectional
- 3-State Outputs
- Linear "On" Resistance
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range.

### MAXIMUM RATINGS\* (Voltages Referenced to V<sub>SS</sub>)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage	- 0.5 to + 18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage (DC or Transient)	- 0.5 to V <sub>DD</sub> + 0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient), per Pin	± 10	mA
P <sub>D</sub>	Power Dissipation, per Package†	500	mW
T <sub>stg</sub>	Storage Temperature	- 65 to + 150	°C
T <sub>L</sub>	Lead Temperature (8-Second Soldering)	260	°C

\* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C

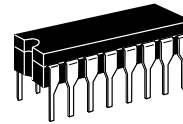
### TRUTH TABLE (X = Don't Care)

ST <sub>X</sub>	ST <sub>Y</sub>	B	A	Z	W
1	1	0	0	X0	Y0
1	1	0	1	X1	Y1
1	1	1	0	X2	Y2
1	1	1	1	X3	Y3
1	0	0	0	X0	
1	0	0	1	X1	
1	0	1	0	X2	
1	0	1	1	X3	
0	1	0	0	Y0	
0	1	0	1	Y1	
0	1	1	0	Y2	
0	1	1	1	Y3	
0	0	X	X	High Impedance	

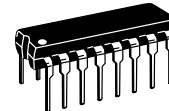
Dual 4-Channel Mode  
2 Outputs

Single 8-Channel Mode  
1 Output  
(Z and W tied together)

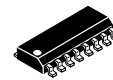
## MC14529B



**L SUFFIX**  
CERAMIC  
CASE 620



**P SUFFIX**  
PLASTIC  
CASE 648



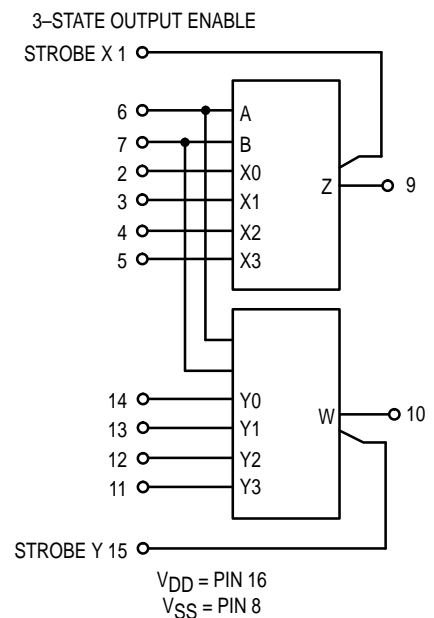
**D SUFFIX**  
SOIC  
CASE 751B

### ORDERING INFORMATION

MC14XXXBCP Plastic  
MC14XXXBCL Ceramic  
MC14XXXBD SOIC

T<sub>A</sub> = - 55° to 125°C for all packages.

### BLOCK DIAGRAM



This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range V<sub>SS</sub> ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>DD</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>). Unused outputs must be left open.

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V <sub>DD</sub>	Test Conditions	- 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ #	Max	Min	Max	

### SUPPLY REQUIREMENTS (Voltages Referenced to V<sub>EE</sub>)

Power Supply Voltage Range	V <sub>DD</sub>	—	V <sub>DD</sub> - 3.0 ≥ V <sub>SS</sub> ≥ V <sub>EE</sub>	3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I <sub>DD</sub>	5.0 10 15	Control Inputs: V <sub>in</sub> = V <sub>SS</sub> or V <sub>DD</sub> , Switch I/O: V <sub>SS</sub> ≤ V <sub>I/O</sub> ≤ V <sub>DD</sub> , and ΔV <sub>switch</sub> ≤ 500 mV**	— — —	1.0 1.0 2.0	— — —	0.005 0.010 0.015	1.0 1.0 2.0	— — —	60 60 120	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package)	I <sub>D(AV)</sub>	5.0 10 15	T <sub>A</sub> = 25°C only (The channel component, (V <sub>in</sub> - V <sub>out</sub> )/R <sub>on</sub> , is not included.)	Typical						(0.07 μA/kHz) f + I <sub>DD</sub> (0.20 μA/kHz) f + I <sub>DD</sub> (0.36 μA/kHz) f + I <sub>DD</sub>	μA

### CONTROL INPUTS — INHIBIT, A, B (Voltages Referenced to V<sub>SS</sub>)

Low-Level Input Voltage	V <sub>IL</sub>	5.0 10 15	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
High-Level Input Voltage	V <sub>IH</sub>	5.0 10 15	R <sub>on</sub> = per spec, I <sub>off</sub> = per spec	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	V
Input Leakage Current	I <sub>in</sub>	15	V <sub>in</sub> = 0 or V <sub>DD</sub>	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μA
Input Capacitance	C <sub>in</sub>	—		—	—	—	5.0	7.5	—	—	pF

### SWITCHES IN/OUT AND COMMONS OUT/IN — W, Z (Voltages Referenced to V<sub>EE</sub>)

Recommended Peak-to-Peak Voltage Into or Out of the Switch	V <sub>I/O</sub>	—	Channel On or Off	0	V <sub>DD</sub>	0	—	V <sub>DD</sub>	0	V <sub>DD</sub>	V <sub>p-p</sub>
Recommended Static or Dynamic Voltage Across the Switch** (Figure 5)	ΔV <sub>switch</sub>	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V <sub>OO</sub>	—	V <sub>in</sub> = 0 V, No Load	—	—	—	10	—	—	—	μV
ON Resistance	R <sub>on</sub>	10 15	ΔV <sub>switch</sub> ≤ 500 mV**, V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control), and V <sub>in</sub> = 0 to V <sub>DD</sub> (Switch)	— —	400 240	— —	120 80	480 270	— —	560 350	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR <sub>on</sub>	10 15		— —	— —	— —	15 10	— —	— —	— —	Ω
Off-Channel Leakage Current (Figure 10)	I <sub>off</sub>	15	V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> (Control) Channel to Channel or Any One Channel		± 100	—	± 0.05	± 100	—	± 1000	nA
Capacitance, Switch I/O	C <sub>I/O</sub>	—	Inhibit = V <sub>DD</sub>	—	—	—	8.0	—	—	—	pF
Capacitance, Common O/I	C <sub>O/I</sub>	—	Inhibit = V <sub>DD</sub>	—	—	—	20	—	—	—	pF
Capacitance, Feedthrough (Channel Off)	C <sub>I/O</sub>	— —	Pins Not Adjacent Pins Adjacent	— —	— —	— —	0.15 0.47	— —	— —	— —	pF

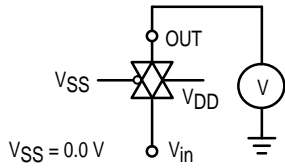
#Data labelled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

\*\* For voltage drops across the switch (ΔV<sub>switch</sub>) > 600 mV (> 300 mV at high temperature), excessive V<sub>DD</sub> current may be drawn; i.e. the current out of the switch may contain both V<sub>DD</sub> and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

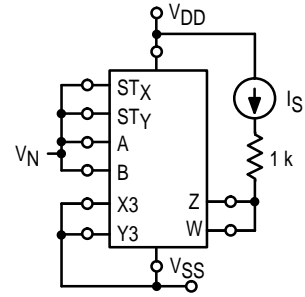
**SWTCHING CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ )

Characteristic	Figure	Symbol	V <sub>SS</sub>	V <sub>DD</sub>	Min	Typ #	Max	Unit
V <sub>in</sub> to V <sub>out</sub> Propagation Delay Time (C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1.0 kΩ)	7	t <sub>PLH</sub> , t <sub>PHL</sub>	0.0	5.0 10 15	— — —	20 10 8.0	40 20 15	ns
Propagation Delay Time, Control to Output, V <sub>in</sub> = V <sub>DD</sub> or V <sub>SS</sub> (C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1.0 kΩ)	8	t <sub>PLZ</sub> , t <sub>PZL</sub> , t <sub>PHZ</sub> , t <sub>PZH</sub>	0.0	5.0 10 15	— — —	140 70 50	400 160 120	ns
Crosstalk, Control to Output (C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1.0 kΩ R <sub>out</sub> = 10 kΩ)	9	—	0.0	5.0 10 15	— — —	5.0 5.0 5.0	— — —	mV
Control Input Pulse Frequency (C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1.0 kΩ)	10	f <sub>in</sub>	0.0	5.0 10 15	— — —	5.0 10 12	2.5 6.2 8.3	MHz
Noise Voltage (f = 100 Hz)	11, 12	—	0.0	5.0 10 15  5.0 10 15	— — —  — — —	24 25 30  12 12 15	— — —  — — —	nV/ √cycle
Sine Wave Distortion (V <sub>in</sub> = 1.77 Vdc RMS Centered @ 0.0 Vdc, R <sub>L</sub> = 10 kΩ, f = 1.0 kHz)	—	—	- 5.0	5.0	—	0.36	—	%
Off-Channel Leakage Current (V <sub>in</sub> = + 5.0 Vdc, V <sub>out</sub> = - 5.0 Vdc) (V <sub>in</sub> = - 5.0 Vdc, V <sub>out</sub> = + 5.0 Vdc) (V <sub>in</sub> = + 7.5 Vdc, V <sub>out</sub> = - 7.5 Vdc) (V <sub>in</sub> = - 7.5 Vdc, V <sub>out</sub> = + 7.5 Vdc)	—	I <sub>off</sub>	- 5.0 - 5.0 - 7.5 - 7.5	5.0 5.0 7.5 7.5	— — — —	± 0.001 ± 0.001 ± 0.0015 ± 0.0015	± 125 ± 125 ± 250 ± 250	nA
Insertion Loss (V <sub>in</sub> = 1.77 Vdc RMS centered @ 0.0 Vdc, f = 1.0 MHz) I <sub>loss</sub> = 20 Log <sub>10</sub> (V <sub>out</sub> /V <sub>in</sub> ) (R <sub>L</sub> = 1.0 kΩ) (R <sub>L</sub> = 10 kΩ) (R <sub>L</sub> = 100 kΩ) (R <sub>L</sub> = 1.0 MΩ)	13	—	- 5.0	5.0	— — — —	2.0 0.8 0.25 0.01	— — — —	dB
Bandwidth (- 3 dB) (V <sub>in</sub> = 1.77 Vdc RMS centered @ 0.0 Vdc) (R <sub>L</sub> = 1.0 kΩ) (R <sub>L</sub> = 10 kΩ) (R <sub>L</sub> = 100 kΩ) (R <sub>L</sub> = 1.0 MΩ)	—	BW	- 5.0	5.0	— — — —	35 28 27 26	— — — —	MHz
Feedthrough and Crosstalk 20 Log <sub>10</sub> (V <sub>out</sub> /V <sub>in</sub> ) = - 50 dB (R <sub>L</sub> = 1.0 kΩ) (R <sub>L</sub> = 10 kΩ) (R <sub>L</sub> = 100 kΩ) (R <sub>L</sub> = 1.0 MΩ)	—	—	- 5.0	5.0	— — — —	850 100 12 1.5	— — — —	MHz

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



**Figure 1. Output Voltage Test Circuit**

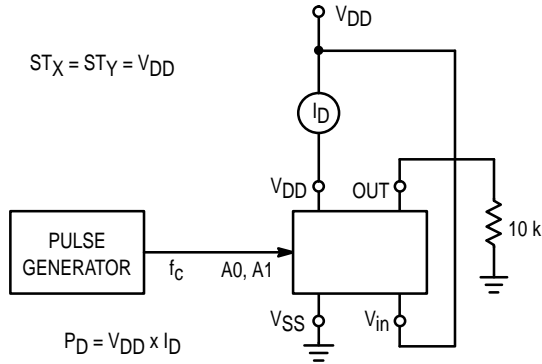


Pins 2, 3, 4, 12, 13 and 14 are left open.

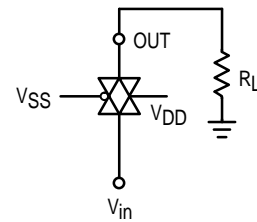
$V_{IL}$ :  $V_C$  is raised from  $V_{SS}$  until  $V_C = V_{IL}$ .  
at  $V_C = V_{IL}$ :  $I_S = \pm 10 \mu A$  with  $V_{in} = V_{SS}$ ,  $V_{out} = V_{DD}$   
 $V_{in} = V_{DD}$ ,  $V_{out} = V_{SS}$ .

$V_{IH}$ : When  $V_C = V_{IH}$  to  $V_{DD}$ , the switch is ON and the  $R_{ON}$  specifications are met.

**Figure 2. Noise Immunity Test Circuit**

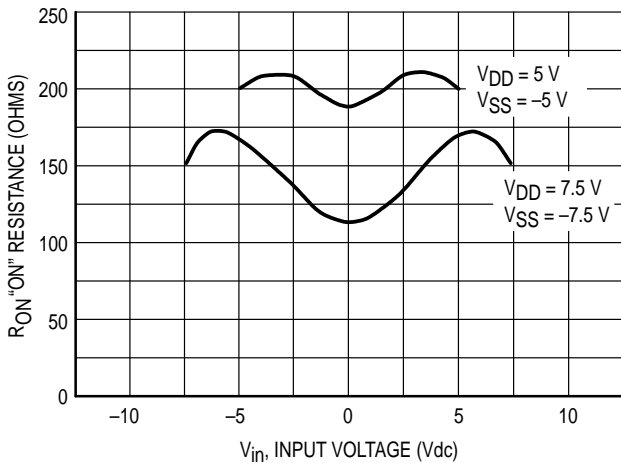


**Figure 3. Quiescent Power Dissipation Test Circuit**

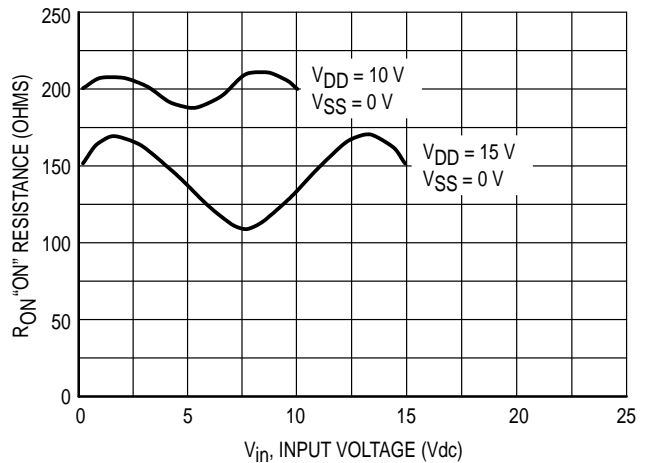


**Figure 4.  $R_{ON}$  Characteristics Test Circuit**

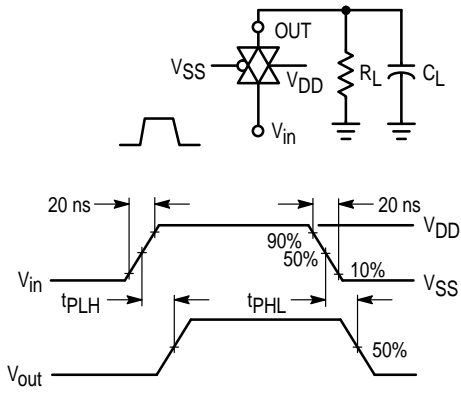
### TYPICAL $R_{ON}$ versus INPUT VOLTAGE



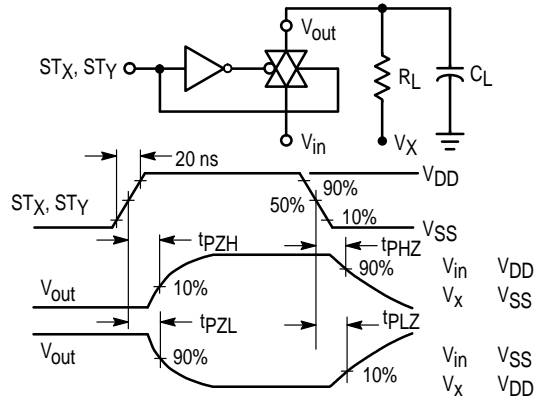
**Figure 5.**



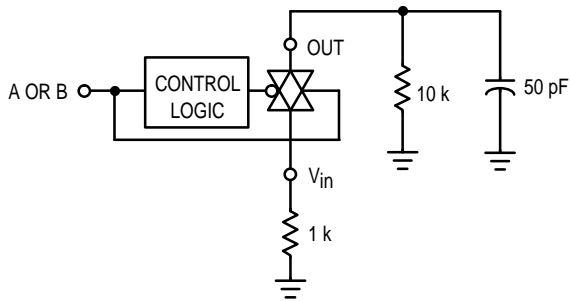
**Figure 6.**



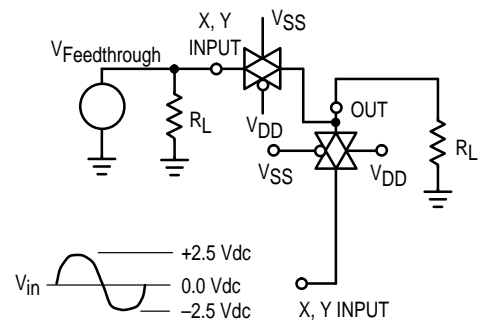
**Figure 7. Propagation Delay Test Circuit and Waveforms**



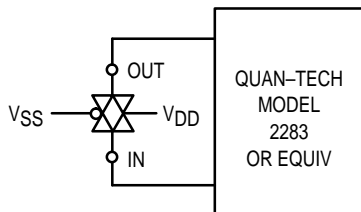
**Figure 8. Turn-On Delay Time Test Circuit and Waveforms**



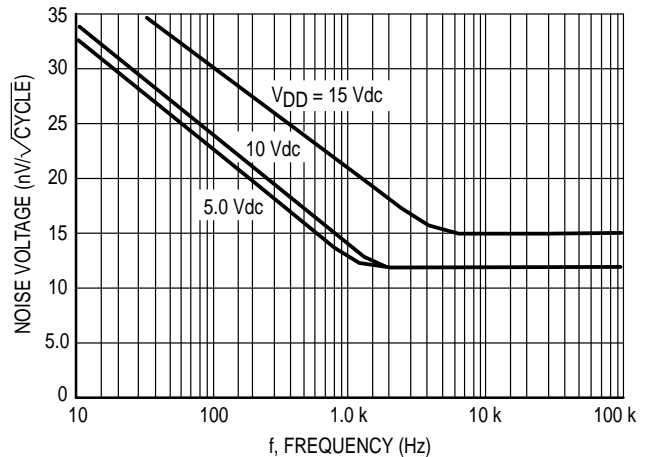
**Figure 9. Crosstalk Test Circuit**



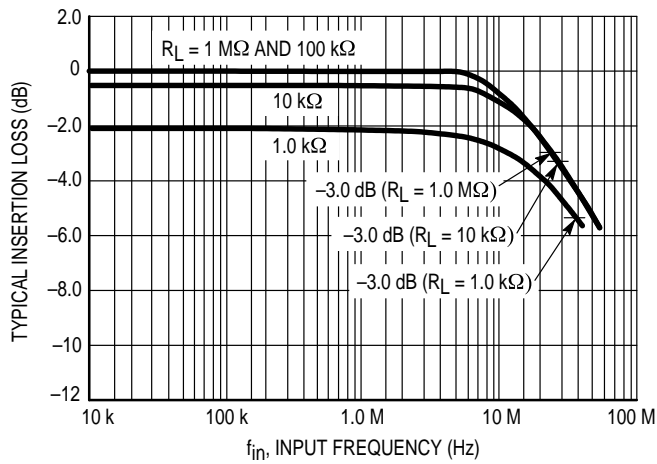
**Figure 10. Frequency Response Test Circuit**



**Figure 11. Noise Voltage Test Circuit**



**Figure 12. Typical Noise Characteristics**

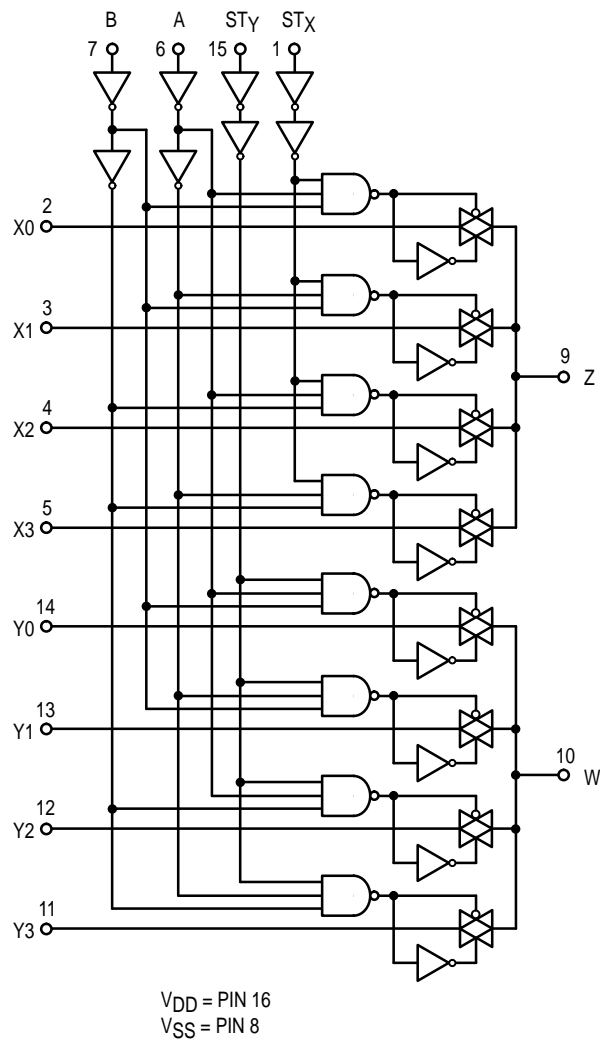


**Figure 13. Typical Insertion Loss/Bandwidth Characteristics**

**PIN ASSIGNMENT**

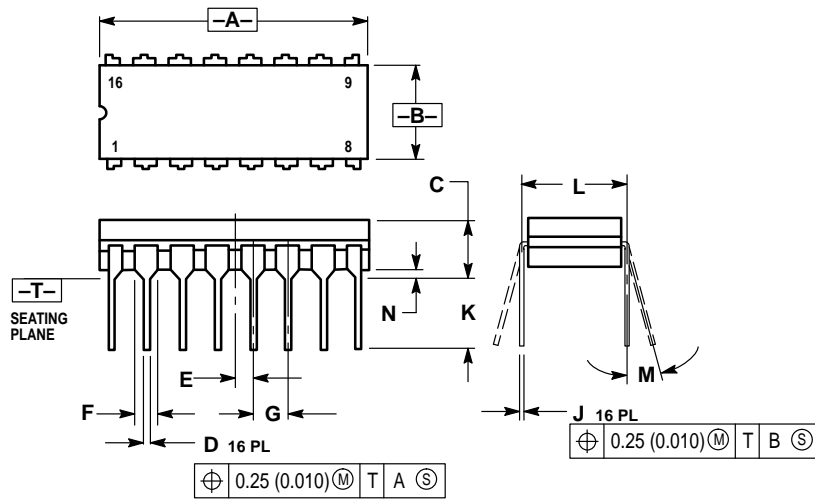
STX	1 ●	16	VDD
X0	2	15	STY
X1	3	14	Y0
X2	4	13	Y1
X3	5	12	Y2
A	6	11	Y3
B	7	10	W
VSS	8	9	Z

**LOGIC DIAGRAM**



## OUTLINE DIMENSIONS

### L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V

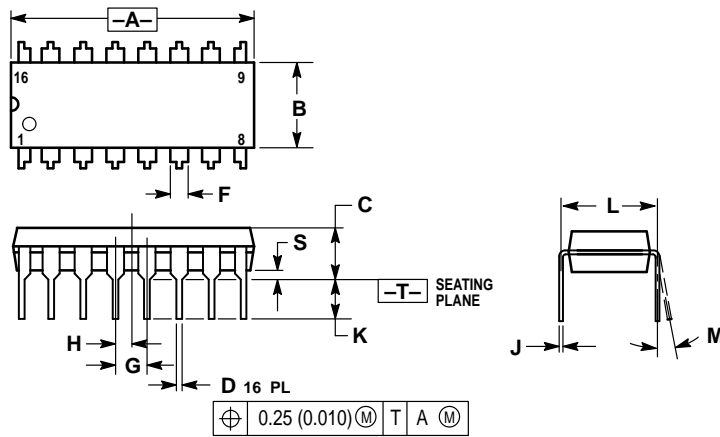


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
<b>A</b>	0.750	0.785	19.05	19.93
<b>B</b>	0.240	0.295	6.10	7.49
<b>C</b>	—	0.200	—	5.08
<b>D</b>	0.015	0.020	0.39	0.50
<b>E</b>	0.050 BSC		1.27 BSC	
<b>F</b>	0.055	0.065	1.40	1.65
<b>G</b>	0.100 BSC		2.54 BSC	
<b>H</b>	0.008	0.015	0.21	0.38
<b>K</b>	0.125	0.170	3.18	4.31
<b>L</b>	0.300 BSC		7.62 BSC	
<b>M</b>	0°	15°	0°	15°
<b>N</b>	0.020	0.040	0.51	1.01

### P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



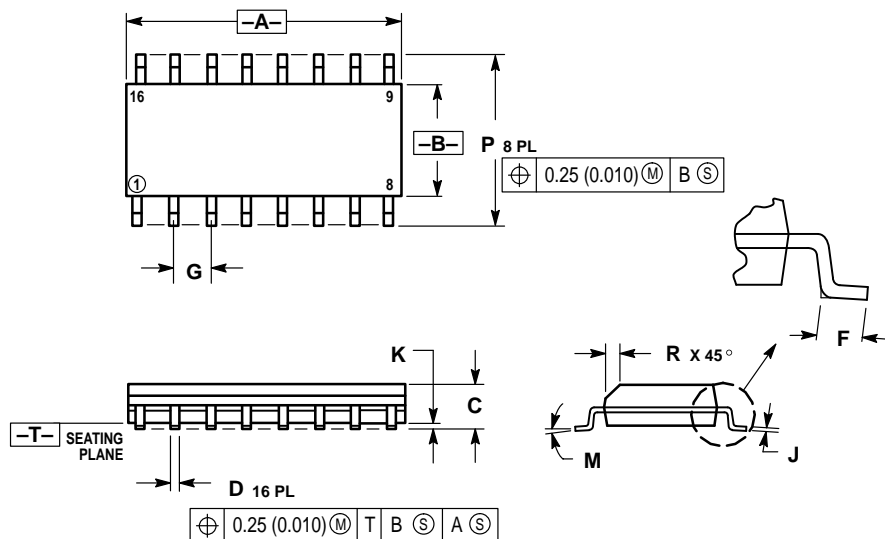
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
<b>A</b>	0.740	0.770	18.80	19.55
<b>B</b>	0.250	0.270	6.35	6.85
<b>C</b>	0.145	0.175	3.69	4.44
<b>D</b>	0.015	0.021	0.39	0.53
<b>F</b>	0.040	0.70	1.02	1.77
<b>G</b>	0.100 BSC		2.54 BSC	
<b>H</b>	0.050 BSC		1.27 BSC	
<b>J</b>	0.008	0.015	0.21	0.38
<b>K</b>	0.110	0.130	2.80	3.30
<b>L</b>	0.295	0.305	7.50	7.74
<b>M</b>	0°	10°	0°	10°
<b>S</b>	0.020	0.040	0.51	1.01

## OUTLINE DIMENSIONS

### D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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MC14529B/D

